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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,500	04/23/2001	Roger S. Tsai	12-1128	4458

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PATENT ADMINISTRATOR
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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	**PAPER NUMBER**
2121	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/840,500	TSAI, ROGER S.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 were examined.

Section I: Non-Final Rejection

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-4 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koh et al., (US Patent 5,878,053; hereafter Koh) in view of Pfeifer et al., titled, "Fabrication and Characterization of Freely Positionable Silicon-On-Sapphire Photoconductive Probes" (hereafter Pfeifer) in further view of Fan et al., (US Patent 5,467,291, hereafter Fan).

Per claims 1, 2,3, 6,7,9, and 10

Koh teaches

- method for modeling one or more predetermined characteristics of a semiconductor (abstract)
- a semiconductor (abstract) device;
- testing the semiconductor (abstract) device;
- to establish a physically representative equivalent model (abstract)
- of said one or more characteristics of said semiconductor (abstract) device;
- varying one or more of said predetermined physical characteristics (i.e. voltage drops, equivalent circuit, etc. abstract)
- one or more predetermined physical characteristics of said semiconductor (abstract) device
- device to establish a revised physically analytical representative model of said semiconductor (Koh: abstract) device

But Koh fails to teaches fabrication and testing of a wafer.

Pfeifer teaches fabrication and the testing of a wafer.

- fabricating (abstract)
- measuring ("measuring modern electronic devices" pg. 2547, Introduction, left column, 2nd paragraph, line 4));
- device with said varied physical characteristics (examples of various dimensions, pg.2547, figures 1 and 2);

- testing of the sample ("test wafer" pg. 2548, left column, line 12) to establish corrected physically representative model.
- For the purpose of rendering PC sampling much more flexible (pg. 2547, left column, last three lines to the first line of the right-hand column)

Fan teaches the motivation for measured data (column 6, lines 1-16)

Therefore it would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify Koh in view of Pfeiffer to use measured data as taught by Fan to faithfully respect the performance of the actual active semiconductor device or circuit over a broad range of operating frequencies large-signal amplitudes levels and operating points.

Per claim 2

Pfeifer teaches

- the varied dimensions (examples of various dimensions, pg.2547, figures 1 and 2)

Per claim3

Pfeifer teaches

- a scanning electron microscope (SEM) (pg. 2548, left column, line 11) is used to measure said predetermined dimensions in step (b).

Per claim 4

Pfeifer teaches

- includes taking S-parameter measurements (pg. 2548, left column, line 11)

Koh teaches

- semiconductor (abstract) device.

Per claim 7

Pfeifer teaches

- measured by way of a SEM (pg. 2548, left column, line 11).

Per claims 8 and 11

Pfeifer teaches

- physically representative model is corrected based upon S-parameter measurements (pg. 2548, left column, line 11).

Per claim 12

Pfeifer teaches

- measurement by way of a scanning electron microscope (pg. 2548, left column, line 11).

5. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Koh as modified by Pfeifer and Fan as applied to claim 1 above, and further in view of Ishimaru

et al., titled "Mechanical Stress Induced MOSFET Punch-through and Process Optimization for Deep Submicron TEOS-O3 Filled STI Device" (hereafter Ishimaru).

Koh as modified by Pfeifer and Fan teaches most of the instant invention as applied to claim 1 above; however, Koh as modified by Pfeifer and Fan, fails to teach semiconductor processing, scaling, bias, temperature and device layout.

Ishimaru teaches semiconductor processing (dependence), scaling, bias, temperature and device layout

- predetermined characteristics include device scaling (pg. 123, right column, "Process Optimization" section, lines 20-23);
- bias dependence (pg. 124 figure 2b "Reverse Bias");
- temperature(pg. 124 figures 5 and 6) dependence;
- lay out (pg. 123, right column, 2nd paragraph, line 15) dependence
- process (Ishimaru: title and Introduction, left column, 1st paragraph, line 9) dependence.

Therefore it would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to execute scaling down the shallow trench (STI) device dimensions for achieving lower mechanical stress and higher manufacturability (Ishimaru: pg. 123, right column, "Process Optimization" section, lines 20-23).

Section II: Response to Arguments

Prima facie

6. Applicant is thanked for responding to this issue. Applicant argues that the 103 fails to provide a prima facie case argument for Koh in view of Pfeifer. The motivation statement has been modified by the inclusion of Fan as set forth above.

Koh/ Pfeifer

7. Applicant argues that neither reference teaches nor suggest a method for developing a physical analytical model to which the Office refutes since Pfeifer teaches a physical ("test wafer", Pfeifer: pg. 2548, left column, lines 10-12) ,analytical model (i.e. simulation model, Koh: column 2, lines 30-33).

Ishmaru

8. Applicant argues that the Ishmaru reference doesn't "really relate to an analytical model of a semiconductor but rather a solution to a mechanical stress problem" (applicants response, pg 5, 2nd paragraph, 8-10). In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Secondly, as stated previously, Koh does teach a analytical model (i.e. simulation model, Koh: column 2, lines 30-33). The rejection, as stated above, stands.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- US 6301510 teaches a method and apparatus for calibrating a semi-empirical process simulator used to determine process values in a plasma process for creating a desired surface profile on a process substrate includes providing a test model which captures all mechanisms responsible for profile evolution in terms of a set of unknown surface parameters.

- US 6223144 B1 teaches a microcontroller software testing tool is disclosed for testing and debugging software for a semiconductor circuit. The microcontroller software testing tool includes a simulator for simulating the execution of the software program on the target semiconductor circuit and an emulator to permit emulation before the actual silicon exists.

- US 5668029A teaches a process for fabricating multi-level semiconductor ROM devices is disclosed. Each memory cell of the ROM device can be programmed to any of three possible conduction states including full-conduction, half-conduction and no-conduction. The fabrication process begins with a semiconductor silicon substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (7:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

Anthony Knight
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Tech Center 2100